REMARKS/ARGUMENTS

Claims 1-2 and 4-7 remain pending. Claim 1 is amended, and claim 3 canceled, by the instant response.

Claim Rejections Based Upon the Hiramuta Patent

In a previous office action, the Examiner rejected claims 1-7 as obvious based upon U.S. patent no. 6,111,312 to Hirumuta et al. ("the Hirumuta patent"), considered in combination with a number of other references. The Hirumuta patent qualifies as prior art to the instant application under 35 U.S.C. 102(e), with an effective priority date of June 2, 1999. The Hirumuta patent issued on August 29, 2000, less than one year prior to the June 29, 2001 filing date of the instant nonprovisional application. Accordingly, in response to the previous office action, a declaration under 37 C.F.R. 1.131 of co-inventor Richard K. Williams was submitted to evidence invention prior to the effective date of the Hiramuta patent.

Now, in the latest office action, the Examiner has maintained rejection of claims 1-7 based upon the Hiramuta patent. Specifically, the Examiner has indicated that while the original declaration is sufficient to demonstrate conception prior to June 2, 1999, it is insufficient to demonstrate diligence over the period of June 2, 1999 - May 15, 2001, the priority date of the provisional application.

Accordingly, filed herewith please also find a declaration under 37 C.F.R. 1.131 of co-inventor James A. Harnden. This declaration provides written documentation of diligent reduction to practice of the instant application over the period June 1999 - May 2001. In particular, attached to Mr. Harnden's declaration are a number of drawings and other documents created during the relevant time period, which show continued work to develop the invention.

Based upon the accompanying declaration of James A. Harnden, considered in conjunction with the previously-submitted declaration of Richard K. Williams, it is respectfully asserted that the Hirumuta patent is not eligible as prior art to the pending claims, as the subject matter of the pending claims was conceived prior to the June 2, 1999 effective date of that reference and diligently reduced to practice thereafter. The instant claim rejections based upon the Hirumuta patent should accordingly be withdrawn by the Examiner.

Claim Rejections Based Upon the Munos Patent

The Examiner has separately rejected certain of the pending claims as obvious based upon U.S. patent no. 6,242,800 to Munos et al. ("the Munos patent"), considered in combination with a number of other references. These claim rejections are traversed as follows.

The Munos patent relates to a package having leads integral with a diepad in order to provide improved conductance of heat therefrom. As conceded by the Examiner however, the Munos patent fails to teach or suggest leads having the specific orientation described in the claims.

In an attempt to provide such a teaching, the Examiner has combined the Munos patent with either U.S. patent no. 5,616,953 to King et al. ("the King patent"), or Japanese patent no. JP359161851A to Yoshida ("the Yoshida patent"). These rejections are overcome as follows.

Regarding the King patent, this reference shows a package featuring a rounded J-shaped lead. As discussed at length in the specification of the instant specification, such a rounded J-shaped lead offers certain disadvantages. One disadvantage is increased vertical profile:

> FIGS. 6A-6E have described and illustrated embodiments of the present invention in connection with a package having lead feet of a J-shape having a uniform radius of curvature. While this lead shape is useful for allocating maximum space efficiency to the package, it does serve to slightly raise the vertical profile of the package. (Emphasis added; page 30, lines 17-20)

Another disadvantage of the rounded J-shaped lead is the difficulty in its formation:

> While a J-shaped lead may be combined with the notch in the package to reduce impact on the package profile height, it is generally more difficult to control the curvature (and hence the height) of a semicircular bend than it is to perform a simple L-shaped bend as shown in FIG. 5A using lead forming (bending) machines in high volume production. (Emphasis added; page 30, lines 21-24)

Embodiments in accordance with the present invention avoid these disadvantages by utilizing a lead having a reverse-gull-wing shape that is angular, rather than rounded:

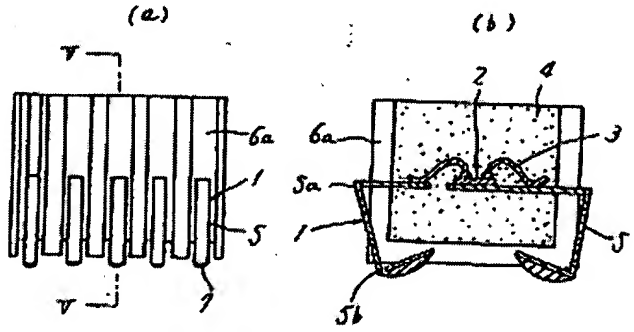
> leads 622 projecting from package body 624 assume a reverse gull wing shape, such that lead feet 622a fold back underneath package body 624 at an angle of incline of between about 4-8° relative to trace 626 of PC board 628. As a result of the angular, rather than rounded, shape of the lead foot, package 620 of FIG. 6F exhibits a vertical profile (Zprofile) that is shorter than that of a package of

equivalent body thickness employing a rounded J-shaped lead foot (Zprofile of FIG. 6E.) (Emphasis added; page 30, lines 26-33)

Claim 1 has now been amended to specify leads having such a reverse gull wing shape.

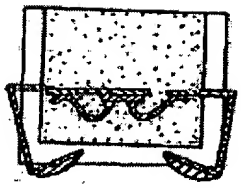
In order to establish a prima facie case of obviousness, the combined prior art references must teach or suggest all of the claim limitations. (MPEP 2143). Here, there is no teaching or even suggestion, in the Munos or King patents taken alone or in combination, regarding a lead having a reverse-gull-wing shape. Accordingly, it is respectfully asserted that the pending claims cannot be considered obvious in light of this combination of references.

Regarding the Yoshida patent, a full English language translation of this reference is provided for the Examiner's reference in the supplemental information disclosure statement filed herewith. Figures 5(a)-(b) of the Yoshida patent shows a package (4) having side grooves (6a) continuous with bottom grooves (6b - referenced but not labeled) running along the entire width of the package at the location of the leads (5) (See page 4, lines 30-31).



Significantly, the Yoshida patent differs from the claimed embodiment in that it shows both the semiconductor pellet (2) and wires (3) positioned on the upper surface of the supporting lead frame (1), away from the lead feet. There is no teaching in the Yoshida patent to position the die on the underside of the leadframe proximate to the lead feet, as is now described in pending independent claim 1.

Moreover, there is no suggestion in the Yoshida patent for such an underside orientation. The following is a diagram of a hypothetical "inverted" version of the package of the Yoshida patent.

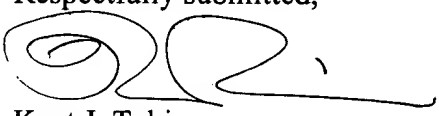


In the above hypothetical "inverted" design of the package of the Yoshida patent, the presence of the groove extending along the full width of the package bottom, risks failing to provide sufficient plastic material to adequately encapsulate the downwardly projecting bond wires. The bond wires are typically relatively fragile package components, and their inadequate encapsulation could expose them to strain and possible fracture.

Again, in order to establish a prima facie case of obviousness, the combined prior art references must teach or suggest all of the claim limitations. (MPEP 2143). Here, there is no teaching or even suggestion in the Munos or Yoshida patents, taken alone or in combination, regarding a package having the die positioned on the underside of the lead frame. Accordingly, it is respectfully asserted that the pending claims cannot be considered obvious in light of this reference combination.

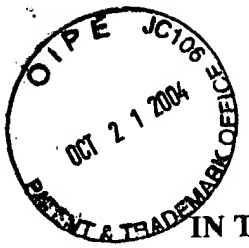
In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance and an action to that end is respectfully requested. If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



Kent J. Tobin
Reg. No. 39,496

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
Tel: 650-326-2400
Fax: 415-576-0300
KJT:ejt
60294445 v1



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Confirmation No. 6536
JAMES HARNDEN et al.	Examiner: Jennifer M. Dolan
Application No.: 09/895,478	Technology Center/Art Unit: 2813
Filed: June 29, 2001	DECLARATION UNDER 37 CFR 1.131 OF JAMES A. HARNDEN
For: IMPROVED SURFACE MOUNT PACKAGE	
Customer No.: 20350	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

I am a co-inventor of the above-referenced patent application, which claims priority from U.S. provisional patent application 60/291,212, filed May 15, 2001 ("the '212 application"). I declare as follows.

1. Attached hereto as Exhibit A is a true and correct copy of an email having the subject line "pdfs", which I received from Phillip Dunning on May 26, 2000. Attached to this email are the following 5 pages of drawings, entitled respectively: 1) "3-5ld"; 2) "Sc70-8j1"; 3) "SC70-8sizeA1"; 4) "Tsop-6j1"; and 5)"Tsop-8jb1". Mr. Dunning was a consultant engaged by GEM Services. The attached drawings are based upon materials created prior to May 26, 2000 and provided to Mr. Dunning, which reflect embodiments of the subject matter of the '212 application.

2. Attached hereto as Exhibit B is a true and correct copy of a document entitled "SC70 MOLD, FORM/SING, ACCEPTANCE", bearing a date of June 5, 2000. This document represents a drawing of an embodiment of subject matter of the '212 application.

3. Attached hereto as Exhibit C is a true and correct copy of a document entitled "TSOP6, 8 LEAD, MOLD, TRIM/FORM ACCEPTANCE", bearing a date of September 14,

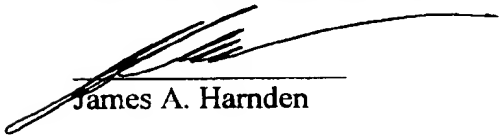
2000. This document represents a drawing of an embodiment of the subject matter of the '212 application.

4. Attached hereto as Exhibit D is a true and correct copy of a document entitled "BACKGROUND FOR 'J-LEAD' PACKAGE". My computer indicated a date stamp of December 27, 2000 for this document. This document represents a draft invention disclosure for the subject matter of the '212 application.

5. Attached hereto as Exhibit E is a true and correct redacted copy of a document entitled "BACKGROUND FOR 'J-LEAD' PACKAGE", dated January 10, 2001. This document represents a revised invention disclosure for the subject matter of the '212 application.

6. Attached hereto as Exhibit F are true and correct copies of three redacted pages of billing records evidencing efforts by Kent J. Tobin to prepare the '212 application between February and May 2001.

I hereby declare that all statements made herein of my own knowledge are true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.



James A. Harnden

10-18-04

Dated

700 Heatherwood Estates Drive
Hollister, CA 95023

Exhibit A
Page 1 of 6

Tobin, Kent J.

From: Philip Dunning [Phil@dunningconsulting.com]
Sent: Friday, May 26, 2000 2:33 PM
To: Jim Harnden
Subject: pdfs

here you are.

I must admit I did not proof themthoroughly, they may have come out in a ugly scale. Pls let me know if you need another try. The 3-5ld one has a scaling problem, but I am not sure what it is meant to look like.

Phil

BACKGROUND FOR "J-LEAD" PACKAGE

PATENT FILING

Background:

New applications are continually requiring lower profile packages and increased efficiency measured in performance/P.C. board area. This increased efficiency demand is takes the form of both, smaller footprints (occupied P.C. board area) for a given performance level, and increased performance for existing footprints. This need exists for both Mosfets and power control I.C.s and covers a range of modern consumer appliances in the portable computer, portable telecommunications and portable entertainment (MP-3 players to digital cameras) markets.

All of the following are independent claims based on packaging technologies and new package designs based on existing packaging technologies. Each may be used independently or in combination with other new or existing designs and technologies to provide height or footprint/performance advantages.

Independent Claims:

1) Micro J-lead package design / configuration

J-lead packages have existed for some time, in the 70s and 80s they were used in "quad" packages (contacts on all four sides) for several MSI products in the 20 to 40 pin count range, for both military and commercial markets. In the 90s, J-lead packages staged a comeback in RAM and Flash memory markets, in even higher pin-counts, as high as 120 pins on large, Quad ("pins on all four sides") packages. Since none of the applications of previous J-lead packages accommodated power devices or vertical conduction discrete devices (Mosfets), several changes were made to improve thermal conduction to the PC board and provide low electrical impedance connections to both sides of the die. Most of these methods are adapted from previous surface mount, "gull-wing lead" packages, such as the SO-8, TSSOP-8 and TSOP-6.

The purpose of the Micro J-lead package: Low-Voltage power applications, such as "electronically controlled switches" for power on/off control of system and sub-system components, and switching components in DC/DC conversion, primarily in battery powered applications like cell phones, portable computers, PDAs, digital cameras, etc.

a) In order to increase the surface mount packages thermal dissipation (over conventional J-lead packages), a copper leadframe material was substituted for more traditional Alloy-42. This is the same concept that has been used to convert SO-8 and TSSOP-8 to Low power applications.

b) To further increase the packages thermal dissipation, all of the leads on one side of the package are directly connected to the die mount pad on which the MOSFET is mounted with thermally conductive epoxy or soft solder. The die pad, or substrate of the die, also serves as the MOSFET Drain connection. This is the same concept used to convert SO-8, TSOP'6 and TSSOP-8 to power MOSFET application.

2) Although the Micro J-lead package demonstrated in illustration "A", achieves the primary objective of increased die area for a given footprint (board area), it does so at the expense or total package height. A significant percentage of customers in the targeted markets are unable to accept packages in excess of the current TSSOP-8 or TSOP-6, which is 1.1mm total height. The body thickness is a complex function of the equipment used to do the assembly, the minimum thickness of the wafers that can be accommodated, and the assembly yield the customer is willing to accept. The thickness of the body has already been optimized to an extent that it can no longer be looked to for any significant savings as a component of total package height.

Claim 1) One of the "unique" changes demonstrated in illustration "B", is in the foot of the leadform for Micro J-lead. It is no longer the traditional "J", but more closely resembles a "reversed-gull-wing" leadform. This allows the foot to maintain an (approximately) 6 degree (with regard to the PC board) incline which promotes solder wetting and allows a point contact with the PC board trace instead of "floating" on the surface of the molten solder during solder reflow.

While this only serves to decrease the total package height slightly, it does adopt a more traditional leadform that has been used to guarantee the lowest electrical resistance path to the board trace, in many previous "gull-wing" leadformed, surface mount power packages.

(Claim 2) To further reduce package height, the "notches", illustrated in drawing "C1" at the bottom of each side of the package body, are a novel and innovative method of allowing the foot of the lead to be recessed as much as 2/3rds of the foot (leadframe) thickness. Since the copper leadframe's minimum thickness is 6 mils, this can account for as much as 4 mils, or 0.1mm, savings in total package height. The two "notches" were allow the leads to be shortened while still providing necessary clearance between the lead and the package body, to avoid interference with solder reflow.

As illustrated in drawing C2, the "notches" are consistent with the internal arrangement of die and leadbonds chosen for the Micro J-Lead packages. This "upside-down" orientation of the die and leadframe was adopted from the TSOP-6, to allow longer and more flexible leads without increasing the total package height, and in this case, to allow the notches to be on the leadbond side of the die. Since the leadbonds are inset, away from the edge of the package, and only on one side of the package, the notches do not violate the 6 mil, minimum coverage design rules of the plastic body material coverage over any of the internal components such as leadframe, die or leadbond.

January 10, 2001
GEM Services, Inc.
(408)566-8859
Jim Harnden

BACKGROUND FOR "J-LEAD" PACKAGE

PATENT FILING

Background:

New applications are continually requiring lower profile packages and increased efficiency measured in performance/P.C. board area. This increased efficiency demand is takes the form of both, smaller footprints (occupied P.C. board area) for a given performance level, and increased performance for existing footprints. This need exists for both Mosfets and power control I.C.s and covers a range of modern consumer appliances in the portable computer, portable telecommunications and portable entertainment (MP-3 players to digital cameras) markets.

All of the following are independent claims based on packaging technologies and new package designs based on existing packaging technologies. Each may be used independently or in combination with other new or existing designs and technologies to provide height or footprint/performance advantages.

Independent Claims:

1) GEM J-lead package design / configuration

J-lead packages have existed for some time, in the 70s and 80s they were used in "quad" packages (contacts on all four sides) for several MSI products in the 20 to 40 pin count range, for both military and commercial markets. In the 90s, J-lead packages staged a comeback in RAM and Flash memory markets, in even higher pin-counts, as high as 120 pins on large, Quad ("pins on all four sides") packages. Since none of the applications of previous J-lead packages accommodated power devices or vertical conduction discrete devices (Mosfets), several changes were made to improve thermal conduction to the PC board and provide low electrical impedance connections to both sides of the die. Most of these methods are adapted from previous surface mount, "gull-wing lead" packages, such as the SC-70 (illustration A) SO-8, TSSOP-8 and TSOP-6.

The purpose of the GEM J-lead package: Low-Voltage power applications, such as "electronically controlled switches" for power on/off control of system and sub-system components, and switching components in DC/DC conversion, primarily in battery powered applications like cell phones, portable computers, PDAs, digital cameras, etc.

a) A J-lead package increases die area for a given footprint by overlapping the die area and the leadbond and leadbond pad isolation areas with the feet of the leads that connect to the PC board as demonstrated in illustration B2. However, the increase in "footprint utilization" comes at the expense of total package height as the spacing inside the packages is the same as it would be for a conventional gull-wing package and the feet are now under-lapping, which raises the package body off the board to provide some room around each lead for solder flow (reflow).

b) In order to increase the surface mount packages thermal dissipation (over conventional J-lead packages) a copper leadframe material was substituted for more traditional Alloy-42. This is the same concept that has been used to convert SO-8 and TSSOP-8 to Low-voltage, power applications.

c) To further increase the packages thermal dissipation, all of the leads on one side of the package are directly connected to the die mount pad on which the MOSFET is mounted with thermally conductive epoxy or soft solder. The die pad, or substrate of the die, also serves as the MOSFET Drain connection. This is the same concept used to convert SO-8, TSOP'6 and TSSOP-8 to power MOSFET application.

2) Although the GEM J-lead package demonstrated in illustration B1, achieves the primary objective of increased die area for a given footprint (board area), it does so at the expense or total package height. A significant percentage of customers in the targeted markets are unable to accept packages in excess of the current TSSOP-8 or TSOP-6, which is 1.1mm total height. The body thickness is a complex function of the equipment used to do the assembly, the minimum thickness of the wafers that can be accommodated, and the assembly yield the customer is willing to accept. The thickness of the body has already been optimized to an extent that it can no longer be looked to for any significant savings as a component of total package height.

Claim 1) one of the "unique" differences from traditional "J" leadforms, demonstrated in illustration "B2", is in the foot of the lead of the GEM J-lead. It is no longer the traditional "J", but more closely resembles a "reversed-gull-wing" leadform. This allows the foot to maintain an (approximately) 6 degree (with regard to the PC board) incline which promotes solder wetting and allows a point contact with the PC board trace instead of "floating" on the surface of the molten solder during solder reflow.

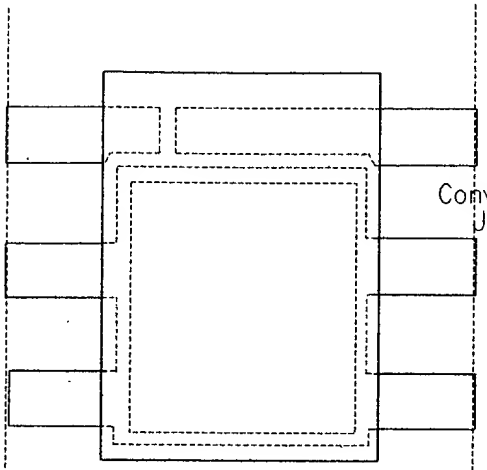
While this only serves to decrease the total package height slightly, it does adopt a more traditional leadform that has been used to guarantee the lowest electrical resistance path to the board trace, in many previous "gull-wing" leadformed, surface mount power packages.

(Claim 2) To further reduce package height, the "notches", illustrated in drawing "B3" at the bottom of each side of the package body, are a novel and innovative method of allowing the foot of the lead to be recessed as much as 2/3rds of the foot (leadframe) thickness. Since the copper leadframe's minimum thickness is 6 mils, this can account

for as much as 4 mils, or 0.1mm, savings in total package height while maintaining the same lead-body clearance. The two "notches" were allow the leads to be shortened while still providing necessary clearance between the lead and the package body to avoid interference with solder reflow.

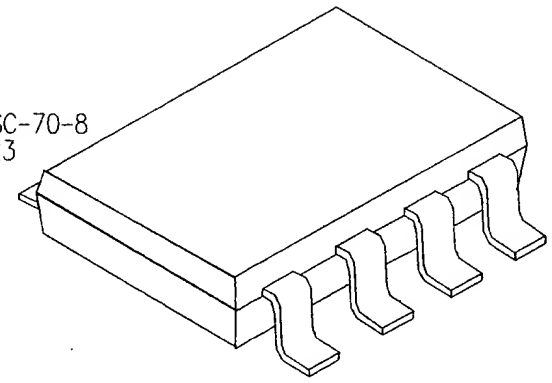
As illustrated in drawing B3, the "notches" are consistent with the internal arrangement of die and leadbonds chosen for the Micro J-Lead packages. This "upside-down" orientation of the die and leadframe was adopted from the TSOP-6, to allow longer and more flexible leads without increasing the total package height, and in this case, to allow the notches to be on the leadbond side of the die. Since the leadbonds are inset, away from the edge of the package, and only on one side of the package, the notches do not violate the 6 mil, minimum coverage design rules of the plastic body material coverage over any of the internal components such as leadframe, die or leadbond.

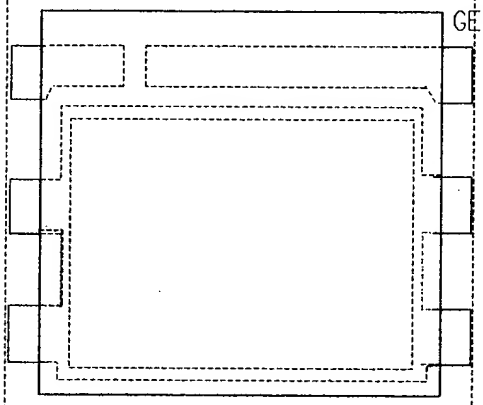
GEM Services, Inc. J-LEAD TECHNOLOGY
Body/die size advantage for existing footprint



Conventional SC-70-8
JEDEC MO-223

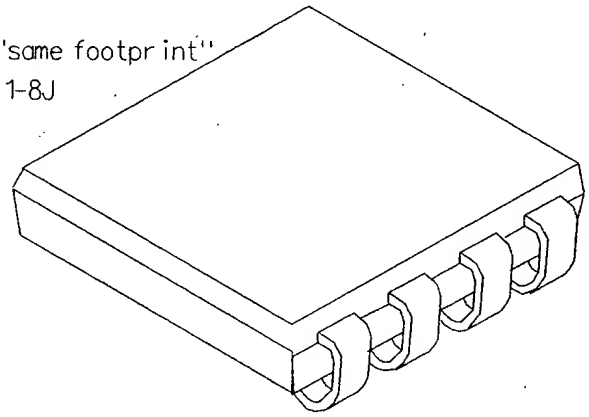
A1

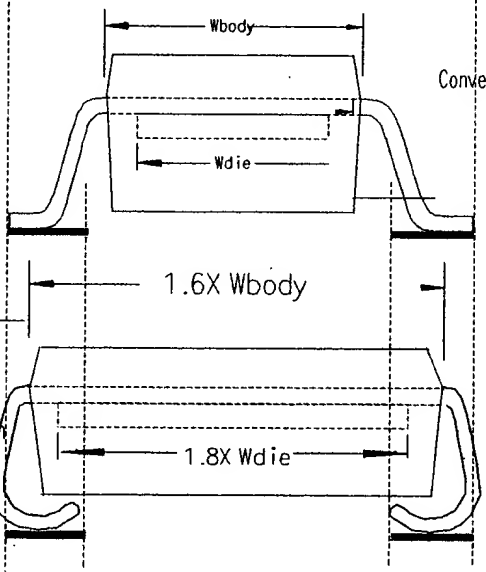




GEM J-Lead "same footprint"
GEM2021-8J

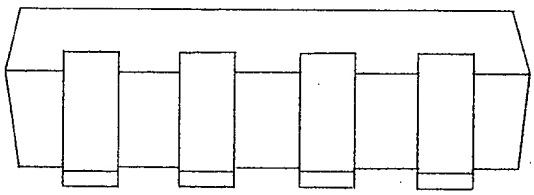
A2





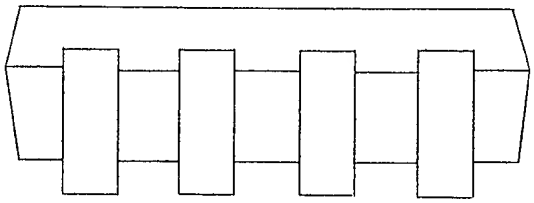
Conventional SC-70

A1

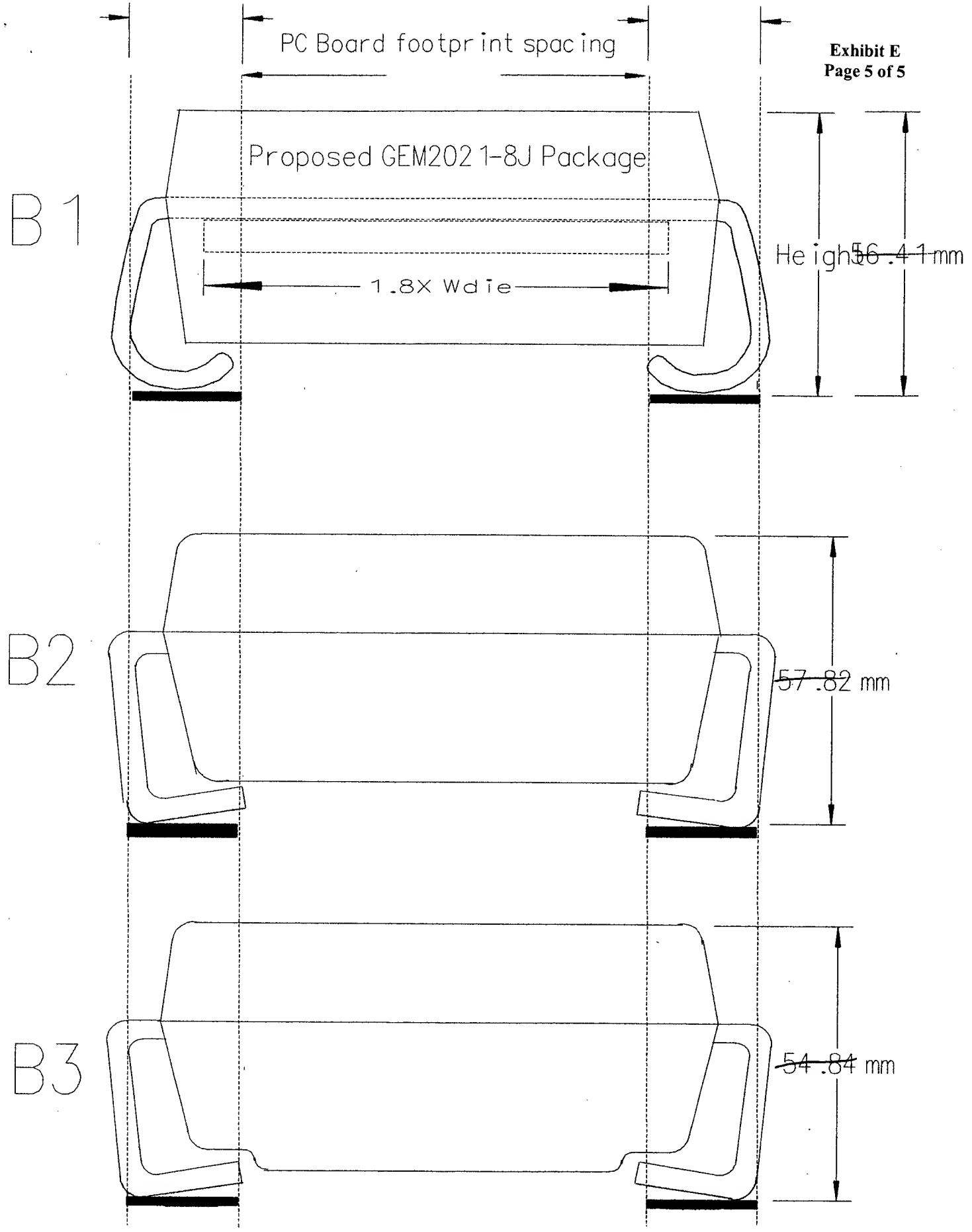


GEM2021-8J

A2



1/9/01 - GEM Services, Inc. - Jim Harnden



1/9/01 - GEM Services, Inc. - Jim Harnden

TOWNSEND AND TOWNSEND AND CREW LLP

GEM Services, Inc.
Attn: James Harnden
1550 Sheffield Avenue
San Jose, CA 95125

Invoice Number 283535
Invoice Date 06/30/01
Client Number 020964-RTO
Matter Number 000200US
Page 3

Re: (000200US) U.S. Patent Utility Electrical
U.S. Patent Application for Improved Surface Mount Package

FOR PROFESSIONAL SERVICES RENDERED:

Date	Aty		Hours	Value
02/21/01	KJT	Receipt and initial review of invention disclosure; initial drafting of patent application.	1.10	
03/19/01	KJT	Drafting of nonprovisional patent application including figures.	3.80	
03/20/01	KJT	Continued drafting of patent application.	1.70	
03/21/01	KJT	Telephone conferences with Mr. Harnden and Mr. Ogawa; continued drafting of nonprovisional patent application.	3.40	
03/22/01	KJT	Continued drafting of nonprovisional patent application including drafting of claims.	2.30	
03/26/01	KJT	Final revision of draft nonprovisional patent application prior to forwarding to Mr. Ogawa for review and comment.	0.70	
04/04/01	KJT	Telephone conference with Mr. Harnden re: status of application and foreign filing options; office conference with Mr. Ogawa re: comments on draft application.	0.60	
04/05/01	KJT	Final revision of draft patent application per the comments of Mr. Ogawa; drafting correspondence to Mr. Harnden forwarding first draft of patent application for review and comment.	3.10	
04/06/01	KJT	Receipt and review of email message from Mr. Harnden re: comments on draft patent application; office conference with Mr. Ogawa re: same; telephone message to Mr. Harnden re: forwarding of additional technical materials.	0.20	
04/09/01	KJT	Telephone conference with Mr. Harnden re: comments on initial draft of patent application.	0.30	
04/11/01	KJT	Telephone conference with Mr. Harnden re: suggested changes to application.	0.50	
04/17/01	KJT	Telephone conference with Mr. Harnden scheduling meeting including Messrs. Ogawa	1.00	

TOWNSEND AND TOWNSEND AND CREW LLP

020964 GEM Services, Inc. Invoice Number 283535
000200US U.S. Patent Application for Improved SurfacPage 4
June 30, 2001

Date	Aty		Hours	Value
		and Williams; research re: foreign and domestic filing of design patent applications.		
04/19/01	KJT	Office conference with Messrs. Ogawa, Harnden, Simmons, and Williams; revision of draft patent application per the comments of Mr. Williams; communication with draftsperson Mr. Giesler re: preparation of design patent applications; drafting email to Mr. Harnden requesting forwarding of electronic files of figures to Mr. Giesler.	8.20	
04/20/01	KJT	Continued revision of patent application per the comments of Mr. Williams.	4.10	
04/23/01	KJT	Continued review and drafting of revised application; telephone conferences with draftsperson Mr. Gielser re: preparation of design patent applications.	4.60	
04/24/01	KJT	Telephone conferences with Messrs. Harnden and Gielser re: design patent drawings; final revision of draft patent application prior to submittal to Mr. Ogawa for review.	6.60	
04/25/01	KJT	Receipt and review of email from Mr. Giesler re: preliminary drawings for three packages; drafting reply email and facsimile showing revised drawing; telephone conference with Mr. Giesler approving corrected drawings.	0.60	
04/30/01	KJT	Receipt of final version of drawings from Mr. Giesler; office conference with Mr. Ogawa re: leadframe design patent; receipt and review of email from Mr. Harnden re: electronic file of leadframe; email and telephone conferences with Mr. Giesler re: same.	0.20	
04/30/01	RTO	Review and revise application	3.50	
05/01/01	KJT	Office conferences with Mr. Ogawa re: comments on draft application; revision of draft application per the comments of Mr. Ogawa; telephone conference with Mr. Harnden re: final approval of design patent drawings for packages.	10.80	
05/02/01	KJT	Office conference with Mr. Ogawa and final revision of draft patent application prior to forwarding to Mr. Harnden and Williams for review; drafting email and facsimile correspondence to Mr. Harnden and Mr. William enclosing draft patent application.	4.10	

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Date	Aty		Hours	Value
05/02/01	RTO	Review and revise application; meet with client	2.50	
05/03/01	KJT	Telephone conference with Mr. Ogawa re: status of application; telephone message to Mr. Williams re: assignment issue; preparation of formal documents to accompany application as filed; refaxing second set of figures to Mr. Williams; telephone conference with Mr. Harnden re: suggested changes; revision of draft application per the comments of Mr. Williams.	3.70	
05/04/01	KJT	Continued revision of patent application per the comments of Mr. Harnden; telephone conference with Mr. Harnden per his comments; forwarding electronic copy of revised patent application to Mr. Harnden and Mr. Williams.	3.40	
05/07/01	KJT	Telephone conference with Mr. Harnden re: comments on second draft of patent application and status of review of same by Mr. Williams; revision of draft patent application per the comments of Mr. Harnden and Mr. Williams.	1.80	
05/08/01	KJT	Telephone conference with Mr. Harnden re: status of review of revised draft of application by Mr. Williams; revision of draft patent application and forwarding of same to Mr. Harnden; drafting facsimile correspondence to Mr. Harnden for review.	0.90	
05/09/01	KJT	Telephone conference with Mr. Harnden re: his latest comments and those of Mr. Simmons on draft patent application; revision of draft patent application per same.	0.70	
05/10/01	KJT	Office conference with Mr. Ogawa re: status of review of application by Mr. Williams; email to Mr. Harnden re: same; drafting email and fax to Mr. Williams forwarding latest copy of draft application.	0.40	
05/15/01	KJT	Telephone conferences with Mr. Ogawa and Mr. Harnden re: filing of application as a provisional application; filing of patent application.	0.80	